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Number	
2.5.7.2	
Subject	
Dielectric Withstanding Voltage (HiPot Method) - Thin Dielectric Layers for Printed Circuit Boards (PCBs)	
Date	Revision
12/07	
Originating Task Group	
Embedded Devices Test Methods Subcommittee (D-54)	

IPC-TM-650
TEST METHODS MANUAL

1 Scope The dielectric withstanding voltage test (HiPot test) consists of the application of a voltage higher than the operating voltage for a specific time across the thickness of the test specimen's dielectric layer. This is used to prove that the PCB can operate safely at its rated voltage and withstand momentary voltage spikes due to switching, surges, and other similar phenomena. Although this test is similar to a voltage breakdown test, it is not intended for this test to cause insulation breakdown. Rather, it serves to determine whether the test specimen's layers have adequate withstanding voltage.

The results can be indicative of a change or a deviation from the normal material characteristics resulting from manufacturing, processing or aging conditions. The test is useful for quality acceptance and in the determination of the suitability of the material for a given application and may be adapted for process control.

2 Applicable Documents

IPC-4821 Specification for Embedded Passive Device Capacitor Materials for Rigid and Multilayer Printed Boards

3 Test Specimens

3.1 Qualification Testing For laminate-like capacitor materials, test specimens **shall** be 50 mm diameter circular (Top Imaged Foil in Figure 1) that **shall** be formed by imaging and then etching the copper foil, unless otherwise agreed by both user and supplier. Spacing between adjacent Top Imaged Foil conductors is recommended to be ≥100 times the dielectric thickness. In order to avoid field gradient and mechanical stress concentration, which can cause faulty dielectric breakdown, the Bottom Foil can be either another larger circle than the Top Imaged Foil or can be a continuous copper sheet. The continuous copper sheet will be required for very thin capacitor dielectric layers that are not self-supporting. At least five test specimens **shall** be tested for qualification.

For nonlaminate like capacitor materials, the test specimen's Top Imaged Foil can be a size other than a 50 mm diameter circle, if this size is not practical or typical. The test specimen's Top Imaged Foil size for these nonlaminate like materials should be set to the largest size normally recommended for this product (see 5.2.4). The thickness for the test specimens should be the typical/recommended thickness. A minimum of five test specimens **shall** be tested for qualification.

3.2 Conformance Testing Test specimens can be the same as used for qualification testing or can be other sizes or shapes. For testing in PCB environments, actual innerlayer power and ground planes can be used. Please note the adjustments for capacitor plate size required in the test procedure (see Section 6).

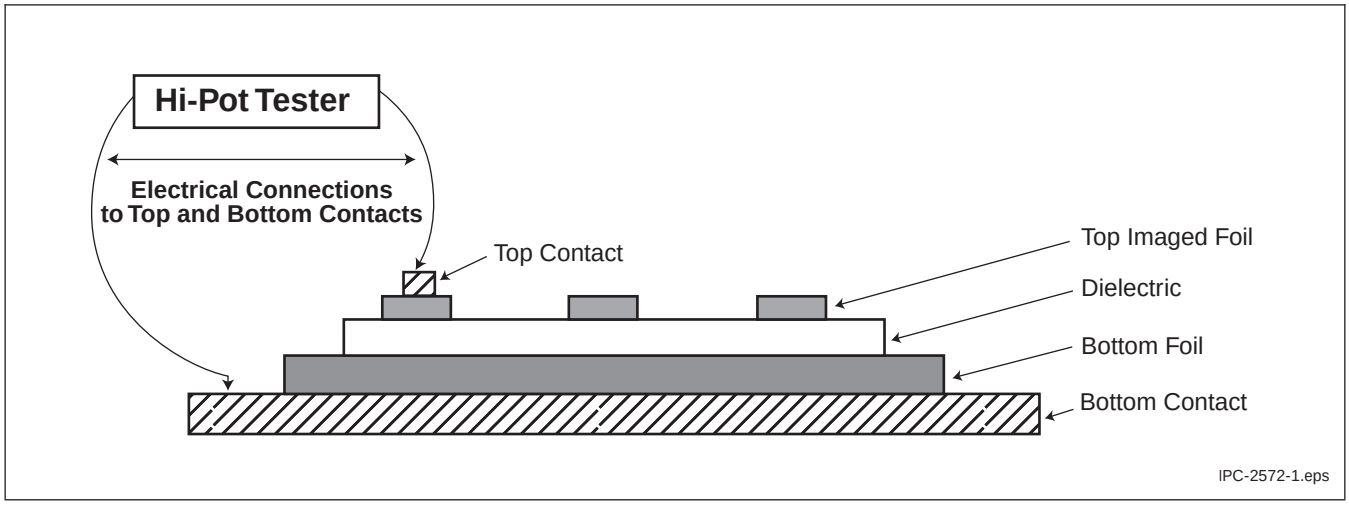

Figure 1 Typical Test Specimen

3.3 Test Specimen Conditioning All qualification test specimens **shall** be conditioned at 23 °C ± 3 °C and 50% ± 10% RH for 24 hours, before testing. For conformance testing, such conditioning is optional.

4 Apparatus

4.1 HiPot Tester A HiPot tester is a piece of equipment capable of supplying a range of DC test voltages appropriate for the materials under test with adjustable ramp rate and hold-time settings. The HiPot equipment **shall** have an adjustable threshold current setting (see 5.4). The user **shall** be satisfied that the HiPot tester is in good working order.

4.2 High Voltage Connections Contacts (conductor plates) apply the voltage from the HiPot equipment to the test specimen's Top Imaged Foil and Bottom Foil (see Figure 1). These contacts should not contain sharp points that could damage either the copper foil or the dielectric layers of the test specimens.

CAUTION: Dangerous voltages may be present on the test connections. Use proper machine guarding and/or machine interlocking.

5 Procedure

5.1 This test method **shall** be performed on fresh test specimens. HiPot testing **shall not** be conducted on test specimens that have previously been exposed to high voltage levels or other similar testing.

5.2 Program the HiPot equipment with the appropriate peak voltage, voltage ramp rate, hold time at peak voltage and current threshold level. Make sure that these values are recorded.

5.2.1 The peak voltage should be as specified in the material Specification Sheet (IPC-4821, *Specification for Embedded Passive Device Capacitor Materials for Rigid and Multilayer Printed Boards*) under the parameter ''HiPot (Volts DC).''

5.2.2 The voltage ramp rate **shall** be 5% of the peak voltage per second, unless otherwise specified.

5.2.3 The hold time at peak voltage **shall** be 30 seconds +3 / -0 seconds.

5.2.4 The threshold settings **shall** be set to a value higher than the in-rush current (due to the charging of the capacitor specimen) observed when the voltage is increased (see 6.1). Many commercial HiPot test instruments display the current during the test. The in-rush current can be determined by setting the threshold current to a high value and then observing the current spikes as the voltage is ramped to the peak voltage. Also note the final, steady-state current during the hold at peak voltage. After several test specimens have been tested and the currents observed, set the threshold current to be greater than the highest current observed.

5.3 The test specimen **shall** be placed between the contacts of the HiPot test equipment (see Figure 1). Start the HiPot sequence.

5.4 Upon completion of the test, the HiPot sequence should include the discharge of the test specimen. (Safety note: Larger test specimens, with high capacitance density, may take more time than expected to discharge.)

5.5 Reporting The HiPot equipment indicates either: Pass or Fail of the material under test (test specimen). A current surge above the threshold current setting indicates a Failure, which may be a result of dielectric failure or manufacturing defects. If the test Passes, record the leakage current per unit area and the passing voltage. If the test Fails, record the failure voltage and threshold current per unit area of each test specimen.

6 Notes

6.1 When the HiPot test instrument voltage changes from one level to the next higher level during the ramp-up to the final voltage, the in-rush current will initially surge above the steady state current because the capacitor is charging. It is possible that this surge in current could exceed the threshold current preset on the HiPot test instrument, causing the instrument to indicate a failure when in fact there was none. The charging current of the capacitor is affected by the change in voltage from one ramp step to another, the dielectric constant of the dielectric, the thickness of the dielectric and the area of the capacitor. High dielectric constant, very thin dielectric thickness and large area of the capacitor plates will all cause the charging current to increase. As a result, the threshold current setting on the HiPot test instrument may need to be adjusted upwards to avoid generating a false failure condition.

6.2 Some thin and filled dielectrics will require a higher threshold current setting, compared to unfilled materials. This

is particularly true of dielectrics containing ferroelectric compounds, such as barium titanate. These materials may show a nonlinear response between current and voltage. At higher voltages, they behave more like resistors than insulators. This is not an issue at most operating voltages, which are normally low, but can be an issue for the HiPot test. At high voltage levels, these materials may trigger a false failure because they allow more current than the threshold setting.

6.3 Some dielectrics may show acceptable HiPot results (ie, ''Pass'') after defects have been ''burned out'' at high voltage (see 5.1).

6.4 Reference Documents

ASTM D149 Dielectric Breakdown Voltage of Solid Electrical Insulating Materials at Commercial Power Frequencies