BUILD ELECTRONICS

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IPC-TM-650
TEST METHODS MANUAL

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Subject	
Measuring High Frequency Signal Loss and Propagation on Printed Boards with Frequency Domain Methods	
Date	Revision
02/2021	
Originating Task Group	
High Frequency Signal Loss Test Methods Task Group (D-24D)	

1 Scope and Purpose

1.1 Scope This document describes the frequency domain test methods to accurately determine the amount of signal propagation loss and delay for electrical printed boards, to meet the demand of high speed applications nowadays. As the data rate of high speed IO continues to increase (e.g., 10 Gbps and above), production testing and development testing require more precise and accurate high frequency methods. (Existing IPC-TM-650 Test Methods such as Method 2.5.5.12A are not adequate). Additionally, previous IPC test methods do not encompass traditional industry methods using VNA, such as thru-reflect-line (TRL), and recent developments of 2X-Thru test methods, etc. This test method is defined to close the gaps.

The scope of this test method includes:

- Calibration and/or de-embedding techniques
- Probing/test fixture choices that impact measurement quality
- Coupon Design
- Test sample pre-conditioning
- Environmental impact, etc.

1.2 Purpose

1.2.1 The importance of Setting up Correct Reference Plane for Printed Board Characterization The importance of setting up a correct reference plane in a typical interconnect measurement setup is illustrated in Figure 1-1. The vector network analyzer (VNA) has been the de-facto standard for accurate passive interconnect characterization including the printed circuit board, connector, cables, etc. Making high quality VNA measurement is straight-forward with standard coaxial connectors and precision SOLT (short, open, load, through) calibration kits. However, test fixtures are usually required to connect the standard coaxial connectors to the non-coaxial device under test (DUT). SOLT calibration can readily move the reference plane to Ref plane A and Ref plane A' in the figure, while the intended DUT is the printed board conductor only (between Ref plane B and Ref plane B'). The test fixtures (between A and B, A' and B') need to be characterized and then de-embedded to recover the insertion loss of DUT.

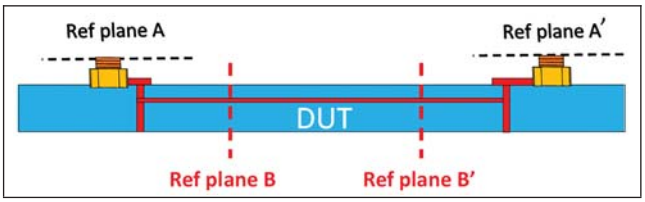

Figure 1-1 Reference Planes in Printed Board Insertion Loss Characterization

Microwave probes are often used to probe interconnect structures for quick measurement, as shown Figure 1-2. A similar calibration or de-embedding procedure is needed to move the reference plane to the target location (Ref plane B and B' shown in the figure). Note that sometimes, an SOLT calibration procedure can be carried out using calibration substrates provided by probe vendor, to move the reference plane to the probe tip, but it does not move the reference plane to the target location and additional de-embedding procedure is still needed.

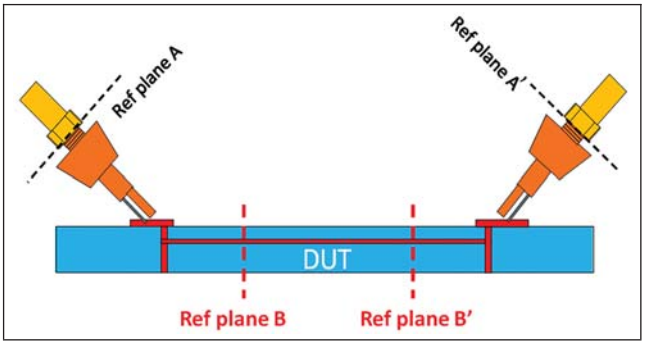

Figure 1-2 Reference Planes in Printed Board Insertion Loss Characterization with Microwave Probe

In a general calibration/de-embedding process, specialized calibration standards with known electrical properties are inserted at the end of the test fixture, and a calibration process is performed to move the reference plane to the end of

the test fixture. The accuracy of the measurement relies highly on the quality of the physical calibration standards, especially for SOLT type of calibration standards, where the parasitics of the SOLT calibration standard must be known a priori. However, for printed board structures, it is not feasible to build an accurate broadband SOLT structure right after the test fixture. Hence the on-board SOLT calibration process usually does not work well above a few GHz.

There are existing calibration/de-embedding methods in the industry for general purpose interconnect characterization to move the calibration reference plane from the coaxial connector to printed board interfaces. These methods are proven by the industry and are applicable to printed board characterization as well. Two of such methods are outlined in 1.3.1 and 1.3.2. However, for the accurate characterization of propagation constant of the uniform transmission line section, simpler and more universal technique can be used as outlined in 1.2.2.

1.2.2 Eigenvalue based De-embedding Methodology for Printed Board Trace Insertion Loss Measurement For printed board trace characterization, there are simple approaches to derive the printed board insertion loss, when the DUT is a uniform transmission line. There are multiple publications proposed that using T-matrix of an ideal transmission line segment can significantly simplify the de-embedding algorithm. The T-matrix is diagonal exponential in the modal space when normalized to the modal characteristic impedance of the transmission line [1]-[6]. If T-matrix of a multi-conductor line segment is converted to S-matrix, the result is an S-parameters (where reference impedance is defined as the characteristic impedance of the transmission line):

$$S_{DUT} = \begin{bmatrix} 0 & e^{-\gamma L} \\ e^{-\gamma L} & 0 \end{bmatrix} \quad \text{(Eq.1)}$$

where γ is the complex propagation constant, and L the line length. An eigenvalue based de-embedding procedure can be carried out utilizing the above assumptions, by measuring S parameters of two different routing lengths. There are various (similar) derivations procedures, and below is one example:

In Figure 1-3, two printed board conductors with different lengths (L1 and L2) are fabricated on the same test coupon.

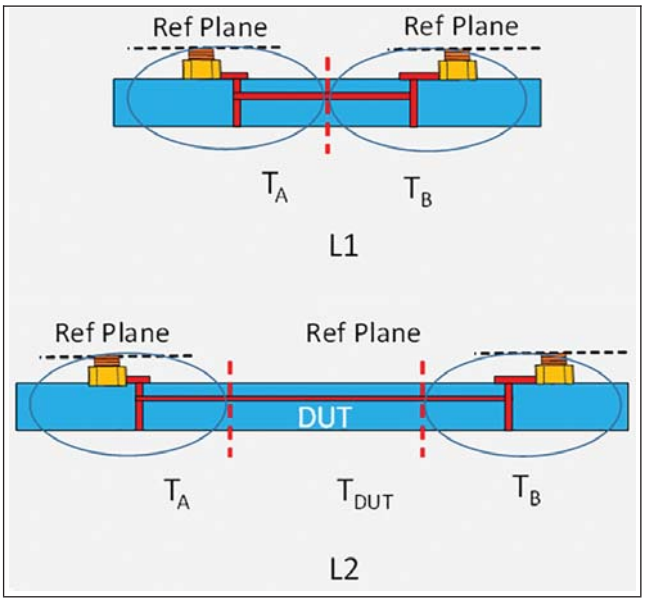

Figure 1-3 Two-line Structure for Eigenvalue-based Method

If we pick the mid-point of L1 structure, and use T-matrices to describe the network parameter of left and right portion of the structure as T_A *and* T_B, then we have

$$T_{L1} = T_A \times T_B \quad \text{(Eq. 2)}$$

$$T_{L2} = T_A \times T_{DUT} \times T_B \quad \text{(Eq. 3)}$$

where DUT is the transmission line with length of L2-L1. From (1) and (2) we can easily get

$$T_{L2} \times T_{L1}^{-1} = T_A \times T_{DUT} \times T_B \times T_B^{-1} \times T_A^{-1} = T_A \times T_{DUT} \times T_A^{-1} \quad \text{(Eq. 4)}$$

Therefore, $T_{L2} \times T_{L1}^{-1}$ and T_{DUT} are similar matrices and should have the same eigenvalue. Meanwhile, assuming the DUT is a uniform transmission line, we have:

$$T_{DUT} = \begin{bmatrix} e^{\gamma(L2-L1)} & 0 \\ 0 & e^{-\gamma(L2-L1)} \end{bmatrix} \quad \text{(Eq.5)}$$

Where γ is the complex propagation constant of the transmission line. There are two eigenvalues of the matrix $T_{L2} \times T_{L1}^{-1}$ (the two non-zero diagonal terms in equation 4), where the one with absolute value <1 is the printed board conductor loss corresponding to the routing length of (L2-L1). Once the eigenvalue is identified, the insertion loss is readily

available based on equation (1). Note that the de-embedded insertion loss is defined with a reference impedance of the transmission line.

1.3 General Calibration/de-embedding Methods to Set up Correct Reference Plane for Printed Board Conductor Insertion Loss Characterization As mentioned earlier, there are existing calibration/de-embedding methods for general purpose interconnect characterization to move the calibration reference plane to printed board interfaces. These methods are validated by the industry, and therefore included herein, although they are either more complicated or costly than the Eigen-value based method.

1.3.1 TRL Calibration The TRL (and its variants such as LRM) method [7] is a general approach to move the calibration reference plane from the coaxial connector to printed board interfaces. Figure 1-4 shows the typical calibration structures for a TRL calibration, with microwave probe footprint (with single-ended probing as an example). The TRL calibration technique only relies on the characteristic impedance of the transmission line and does NOT need the parasitics of Reflective Standard to be known, nor propagation delay of Line. A typical TRL calibration structure may also include a Load structure that works only at very low frequencies, and additional Line structures to cover a wide frequency range.

Most VNAs offer TRL calibration options, please refer to the manual or application note for your specific equipment to perform a TRL calibration.

TRL calibration has been widely used in the industry since the technique no longer requires accurate calibration termination standards. This overcomes the difficulties of SOLT calibration, and the reference plane can be moved to the printed board. However, there are still some disadvantages to the TRL calibration. For example, there are many components of the calibration standard to handle. This takes substantial printed board area and requires tedious calibration process in the lab, while being prone to the operator error. Additionally, the TRL technique requires accurate characteristic impedance specification for the line standard, which is problematic to determine in a dispersive environment.

1.3.2 2X-Thru De-embedding In the last decade, the 2X-thru de-embedding methodology is gaining popularity due to its simplicity of test fixture design and de-embedding procedures [8]. In contrast to the TRL calibration technique, which requires measurement of multiple structures as shown in Figure 1-4, 2X-Thru De-embedding requires only one de-embedding structure.

The basic idea of the 2X-Thru de-embedding approach is shown in Figure 1-5. The S-parameters of the 2X-thru

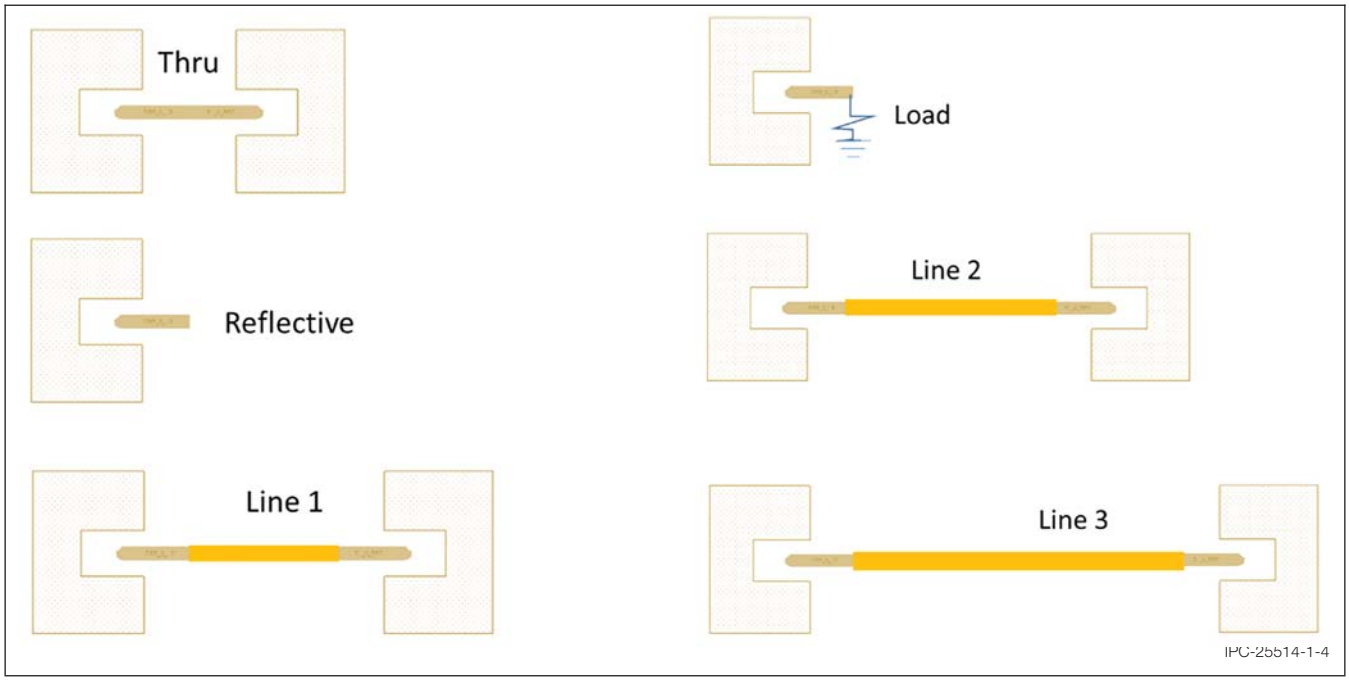

Figure 1-4 Calibration Structures (with probing footprint) for a TRL Calibration Example

structure are measured first. Assuming the 2X-Thru structure is symmetric, the S-parameters of a 1X structure can be calculated directly from the 2X-Thru measurement. Once the S-parameters of the 1X structure on both sides on the DUT are obtained, the S-parameters of the DUT can be readily calculated. This significantly simplifies calibration/de-embedding procedures as compared to a traditional TRL calibration where six calibration structures are typically needed.

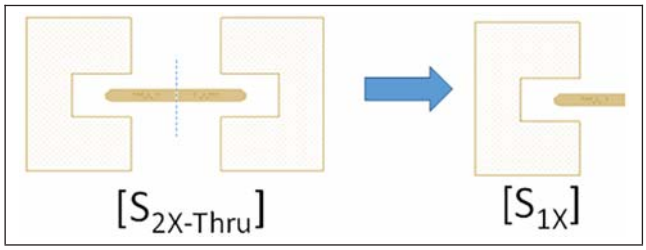

Figure 1-5 S parameter of Test Fixture is Calculated from S Parameter of 2X-Thru

There are various 2X-Thru de-embedding tools available at time of publication of this test method, such as [9][10][11]. The accuracy of 2X-Thru de-embedding tool is has been shown to be comparable to TRL [13]. However, since the algorithm of commercially available 2X-Thru methods are often proprietary, it is up to the users to validate the tool for their printed board insertion loss measurements. IEEE 370-2020 addressing this issue by setting up a process to validate the de-embedding tools [12]. Below is the general process of using 2X-Thru de-embedding process to measure the insertion loss:

1) Manufacture two printed board conductors with different lengths (L1 and L2).
2) Perform SOLT calibration to move reference plane to the end of coaxial connector.
3) Perform VNA measurement and to acquire the S parameters of the shorter conductor (L1) and longer trace (L2).
4) Use 2X-Thru tool to de-embed the S parameters of L2, while treating the shorter conductor L1 as test fixture. This end up with S parameters of a transmission line DUT of length L2-L1.
5) Renormalize the S parameter using the characteristic impedance of transmission line.
6) The renormalized S21 represents the insertion loss of DUT (length of L2-L1).

2 Applicable Documents

IPC-TM-650 Test Methods Manual

2.5.5.12 Test Methods to Determine the Amount of Signal Loss on Printed Boards

3 Test Specimens

3.1 Common Test Coupon Characteristics The test coupon contains two or more transmission lines. The following are general guidelines for designing transmission line test structures for the test methods within this document. These transmission line test structures may be placed within the functional area of the printed board or within test coupons. It is recommended that coupons have labels that contain information about the associated test line signal layer; for example, L1, L3, etc. Labeling of the contact land for differential conductors shall clearly indicate the matched pair. It is recommended that test coupons include a printed board serial number, part number, and date code.

3.2 Ground and Reference Planes All reference planes in the coupon **shall** be connected together within the coupon area and be independent of those planes in the functional circuit area.

3.3 Probe Launch Footprint The probe launch footprint is comprised of signal pads and ground contact. Each probe vendor can specify its optimized probe launch footprint. However, it is desirable to have footprint that is compatible with multiple probes. Figure 3-1 shows an example of a differential probe launch footprint compatible with both micro- and handheld probes. A similar single-ended probe launch footprint is shown in Figure 3-2, with the same guide pin design.

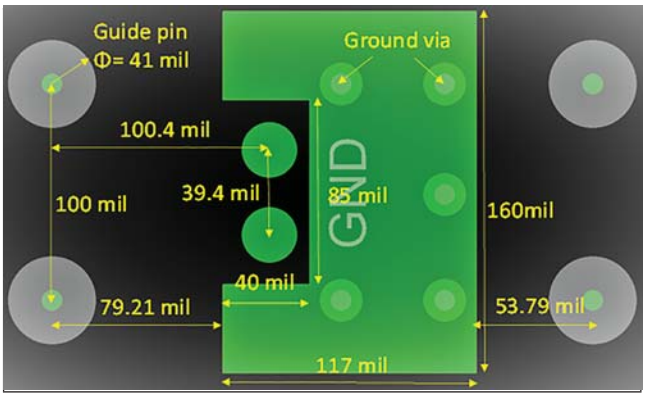

Figure 3-1 Example of a Probe Launch Footprint for Differential Signal Probing (both footprint and dimensions are shown for informative purposes only)

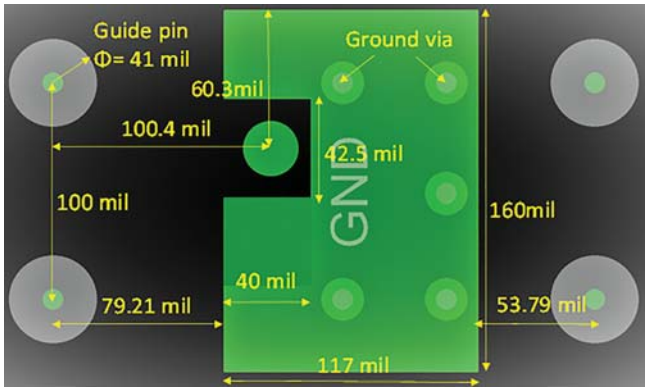

Figure 3-2 Example of a Probe Launch Footprint for Single-ended Signal Probing (both footprint and dimensions are shown for informative purposes only)

It is important to note that these are just footprint examples, and the electrical performance of these footprint may be further improved based on the layer stackup, such as voiding the ground plane right beneath the signal pads. Each probe vendor can specify its optimized probe launch footprint that meets the electrical requirement specified in 4.2. Furthermore, it is critical to work with probe vendor to make sure the finished drill hole size is compatible with the probe.

Note that the footprint example shown in Figure 3-1 is applicable for measurements up to 20GHz and that the footprint can be further optimized for application at higher frequencies.

3.4 Connector Launch Alternative to microwave probes, high bandwidth connector launch may be used instead of probe launch as show in Figure 3-2 and Figure 3-3 of IPC-TM-650 Method 2.2.2.12A. Although the hand-held probe approach is quicker and more convenient to use, the connector solution is usually more reliable and less prone to human errors.

3.5 General Surface Condition The panel test coupons **shall** have the same surface plating and use the same solder mask requirements as the functional printed board. The plating of the launch footprint should be suitable for probing or co-axial connector connection.

3.6 General Routing Guidelines The test lines **shall** be referenced to a continuous ground/voltage planes. The test line conductors **shall** be kept at minimum distance Dmin from printed board structures such as voids, plane splits, other conductors and holes, where Dmin is six times the height of dielectric layer (from line conductor to the closest reference plane) or 2.54 mm [0.100 in], whichever is greater.

Fiber-weave impact should be mitigated unless the intent is to measure its impact. One mitigation example is to have the test line routed at about 10 degree angle (or close to the routing scenario in actual product design) with respect to the fiber-weave alignment. Alternative, straight routing (parallel to board edge) can be used if the Gerber image is rotated by about 10 degrees on the panel.

It is recommended to route the test lines with the same cross-section and target impedance as in the actual product layout.

Thieving, which is the use of non-terminated copper structures such as planes, pads, and/or conductors adjacent to test lines that ensure plating consistency, may be used on the test coupon. All thieving structures (if used) **shall** be placed at least Dmin away from each test interconnect. It is recommended to make sure copper density at each routing layer is representative of the actual product.

3.7 Impact of Vias in the Printed Board Conductor Loss Characterization Measuring the signal loss for inner layer (stripline) can be challenging when there is a substantial loss due to the via or via stub effect. Reducing via effect can improve the de-embedding results. This can be achieved by:

- Minimizing via stub length by probing from the appropriate side of the board (from the top for traces on the bottom half of the board and vice-versa, to assure minimum via stub length)
- Minimizing via stub length by back-drilling. However, this needs to be done with good control of back-drilling depth. Inconsistent back-drilling depth between the vias for two different routing length can lead to large de-embedding error
- Extra attention needs to be paid to stacked via designs, as this approach, while avoiding stubs and improving signal integrity, has high manufacturing variants
- The resonance frequency should be outside of intended measurement bandwidth

For signals on outer layer (microstrip), the conductor should be routed without via or via stub.

3.8 Impact of Environmental Condition in the Printed Board Conductor Loss Characterization Temperature and humidity affect loss measurements. It is therefore critical to clearly document the testing condition in the reported insertion loss.

For insertion loss of conductors routed on outer layer, the results can be different under the conditions described in 3.8.1 vs. those described in 3.8.2 due to the humidity impact.

As the solid metal planes may block the moisture penetration, for the conductors routed on inner layers it typically takes a long time (with rare exceptions) for the sample to absorb the moisture. Therefore, making measurement of insertion loss of inner routing layers under the conditions described in 3.8.1 is recommended over making such measurements under the conditions described in 3.8.2.

3.8.1 Insertion Loss Measurement of Vacuumized Test Specimens Test specimens can be vacuumized right after baking them at 105 °C RH 0% over 2 hours, or 140 °C RH 0% over 1 hour. However, if the coupon has been stored over a long period of time without proper vacuum packaging, the baking condition needs to be adjusted to be 140 °C RH 0% for 12 hours. Consistent results can be obtained by testing specimens at 23 °C (± 2 °C) [73.4 °F (± 3.6 °F)] and 20~80% RH for less than 12 hours since opening the vacuum package or finishing a baking treatment. It is recommended to allow test coupons to cool to room temperature for at least 30 minutes before test if measurement is done after a baking treatment.

3.8.2 Insertion Loss Measurement of Test Specimens Stored in Environmental Chamber For conductors routed on outer layers, consistent results of insertion loss at typical humidity condition can also be obtained by storing test specimens at 23 °C (± 2 °C) [73.4 °F (± 3.6 °F)] and 40% RH (± 5% RH) for no less than 48 hours. Note that the test under this condition takes longer time compared to that described in 3.8.1.

4 Apparatus

4.1 VNA Measurement Apparatus The measurement equipment needed includes a VNA, calibration kit, cabling, and a probing solution, as shown in Figure 4-1. High performance connectors and cables that are rated above the maximum frequency of interest are required in performing VNA measurements.

Using TDR/TDT system in place of a VNA to acquire frequency domain attenuation and loss data is beyond the scope of this test method. A future IPC-TM-650 Test Method 2.5.5.15 for best design practices for Time Domain method is envisioned under the IPC D-24D Task Group.

4.2 Probe Quality The quality of probe (whether using probing station or handheld probe) is critical for accurate and repeatable measurement. It is recommended to have the insertion loss of the probe and launching pad to be less than

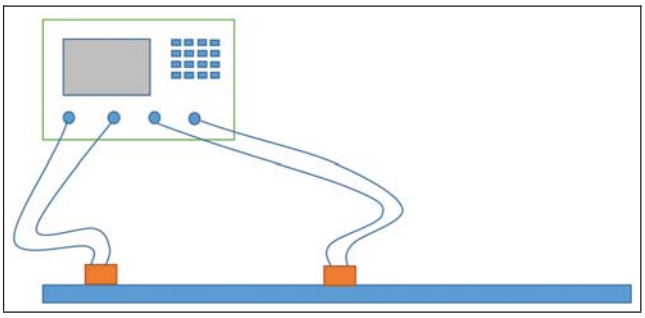

Figure 4-1 Typical VNA Measurement Setup

3.5 dB at highest frequency of interest, to make sure the probe and launching pad design have good electrical performance.

A direct measurement of electrical performance of probe and launching pad can be cumbersome. Alternatively, Figure 4-2 shows an example of test setup to check the electrical performance. A 50.8 mm [2.0 in] microstrip line with known insertion loss is used to provide a connection between two probes. VNA is calibrated to the end of coaxial cable, and the insertion loss of the 50.8 mm [2.0 in] microstrip line with probes at both ends is measured.

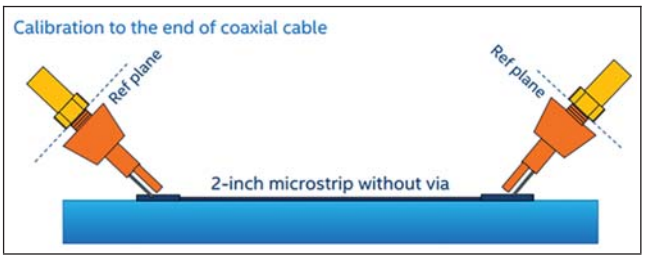

Figure 4-2 Test Setup for Probe Quality Check

Insertion loss requirement for the test setup in Figure 4-2 depends on the highest measurement frequency, as well as the microstrip trace loss. A test coupon with known loss can be used, or a separate measurement can be done to determine microstrip loss. Figure 4-3 shows an example of the probe quality requirement, assuming the highest measurement frequency is 20 GHz, and the insertion loss of the 50.8 mm [2.0 in] microstrip is 5 dB at 20 GHz. The measured insertion loss must be above the red dash line in the figure. Note at DC level, the required loss is less than 1 dB, and at 20 GHz, the required loss is less than12 dB (where 3.5 dB is allocated for each probe, and 5 dB is coming from the 50.8 mm [2.0 in] microstrip).

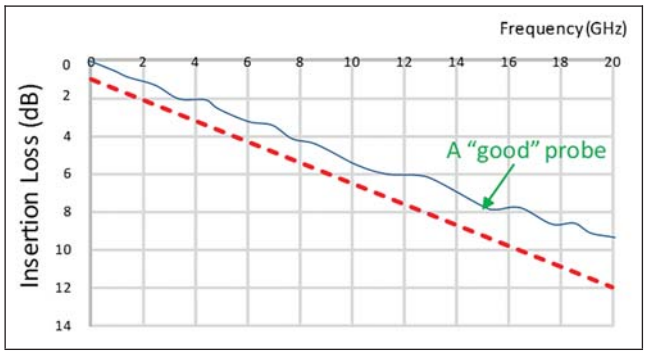

Figure 4-3 Insertion Loss Requirement for the Probe Quality Test Setup in Figure 4-2

Probe performance may degrade over time. It is necessary to periodically check the probe quality to assure the electrical requirement in Figure 4-3 is met.

5 Procedure The procedure section is to be used to detail all of the specific steps necessary to perform the actual test. It **shall** include any specific conditioning requirements, or other specimen preparation not previously detailed. It **shall** then describe in detail the successive steps of the procedure, grouping related operations into logical divisions in a concise manner. It **shall** include times, temperatures, voltages, pressures, concentrations, linear measurements and quantitative criteria when necessary in applicable units (both Metric and English).

It **shall** then state any detailed information required in reporting the test results. When two or more procedures are described in the same test method, the report **shall** indicate which of the procedures was used. When a test method allows variations in operating or other conditions, the report **shall** state the particular conditions utilized for the test.

This specification currently outlines measuring Frequency Domain characteristics using a VNA.

5.1 VNA Settings Follow the VNA manual for proper operation of equipment. Recommended settings for the VNA include an IF bandwidth of 1 kHz (can be decreased based on instrument and applications), and a step size of 10 MHz. Smoothing is not allowed.

The cables and connectors used in the measurement should be sufficiently rated for the maximum intended measurement frequency.

5.2 Conditioning of Test Sample Refer to 3.8 for proper conditioning of test sample before test.

5.3 VNA Calibration and De-embedding Calibration and/or de-embedding techniques outlined in 1.2.1 must be performed to remove the effects of cable, connector, and test fixtures.

5.4 Smoothing and Fitting of Insertion Loss Measurement Curve

5.4.1 Insertion Loss Smoothing Basics Printed board testing facilities often report insertion loss per inch at a handful of frequencies (e.g., 4 GHz, 8 GHz, 12.89 GHz, etc.). An ideal insertion loss curve for a printed board conductor is expected to follow transmission line behavior and be smooth. However, in some testing houses, the de-embedded insertion loss curves may have oscillations and deviations due to various sources of measurement and de-embedding error, as shown in blue curve in Figure 5-1. Without proper post-processing of the data, the measurement house can easily fail to report the true loss performance of the test coupon at designated frequencies. One common methodology for obtaining a smooth de-embedded insertion loss curve is to use an iterated moving average. The result is a very smooth red curve shown in Figure 5-1.

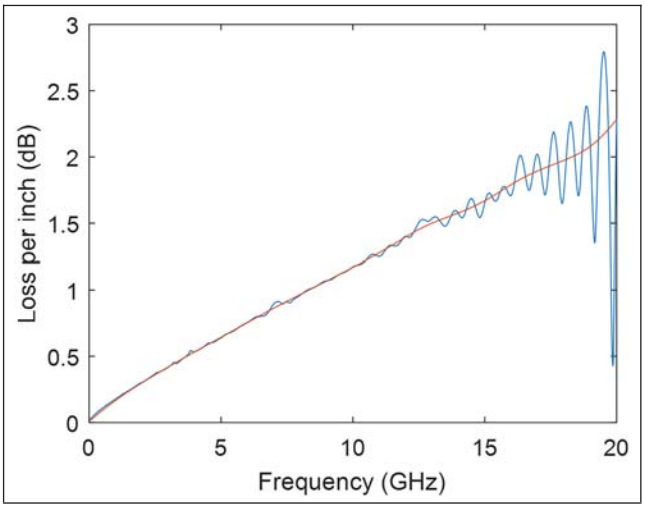

Figure 5-1 An Iterative Moving Average Applied to a Typical Insertion Loss Curve
Note 1. Red denotes the smoothed curve

While smoothing with an iterative moving average addresses most of the challenges posed by the measurement errors, there remain some disadvantages. The resulting smooth curve is non-physical and unlikely to be representative of the true loss of printed board conductor. For example, the smoothed curve usually deviates from the correct answer at low

frequencies where the conductor losses dominate. Additionally, in the high frequency range, the smoothing may preserve unrealistic features of the de-embedded insertion loss.

5.4.2 Cumulative Dielectric and Conductor Loss Fitting As it has been discussed in [14], the cumulative dielectric and conductor losses can be generally approximated by

$$IL_{dB}(f) = a\sqrt{f} + bf + cf^2 \quad \text{(Eq. 6)}$$

where f is the frequency in GHz and a, b and c are constants. For most of the cases coefficient $c << 1$ and can be neglected. Therefore, as a first approximation the total loss curve can be fitted to

$$IL_{dB}(f) = a\sqrt{f} + bf \quad \text{(Eq. 7)}$$

There are number of algorithms that can be used to perform the printed board loss fit to Eq. 7. One of the most well-known and widely available algorithms is the least squares fit, example of which is shown in the Figure 5-2 below.

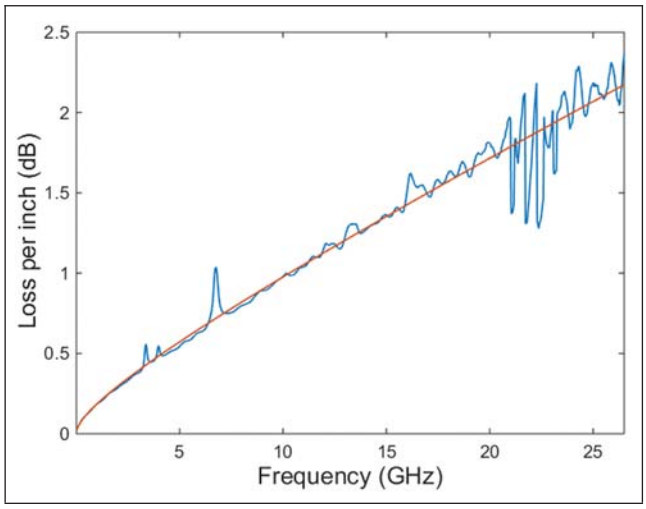

Figure 5-2 Least Squares Fit Based on (eq. 7) Applied to a Representative Insertion Loss Curve
Note 1. Red represents the fitted curve.

Even though least squares generally provide a good curve approximation with the specified behavioral function, there are many other fitting algorithms that can be applied.

5.4.3 An Alternative Cumulative Dielectric and Conductor Loss Fitting Alternatively, when losses cannot be fitted to the conventional physical based behavioral functions in (Eq. 6) and (Eq. 7), especially when measurement raw data has high ringing resonances, other empirical approximations can be used. Fox example, in [15], the following function is set as the target function for the fitting algorithm:

$$IL_{dB}(f) = a(f - f_0)^b + c(f - f_0)^2 + d(f - f_0) + IL_0 \quad \text{(Eq. 8)}$$

The first term represents the AC conductor loss (i.e., the skin-effect losses), where 'b' is an additional fitting parameter (instead of a constant 0.5 where ideal conductor loss is a function of $f^{0.5}$) added to take into account the surface roughness impact of the conductor. The second and the third terms represent dielectric losses, and the constant represents the conductor's DC loss. Furthermore, a certain offset point (f_0, IL_0) is introduced, where f_0 is the first frequency point of the measurement. The offset is added to accommodate the fact that VNA measurements made at the printed board fabricator usually do not provide results lower than 10 MHz.

The abovementioned methods fit the data to a smooth curve over the entire bandwidth of the measurement where each data point is allocated equal weight. As measurement errors usually increase significantly at high frequencies, a weighting scheme can be introduced to force the algorithm to prioritize the curve fitting at the low frequencies and minimize (or ignore) the impact of high frequency:

$$W(f) = \left(1 - \left(\frac{f}{f_{max}}\right)\right)^3 \quad \text{(Eq.9)}$$

where f_{max} is the maximum measurement frequency. Figure 5-3 shows the suggested weighted function where $f_{max} = 20$ *GHz.*

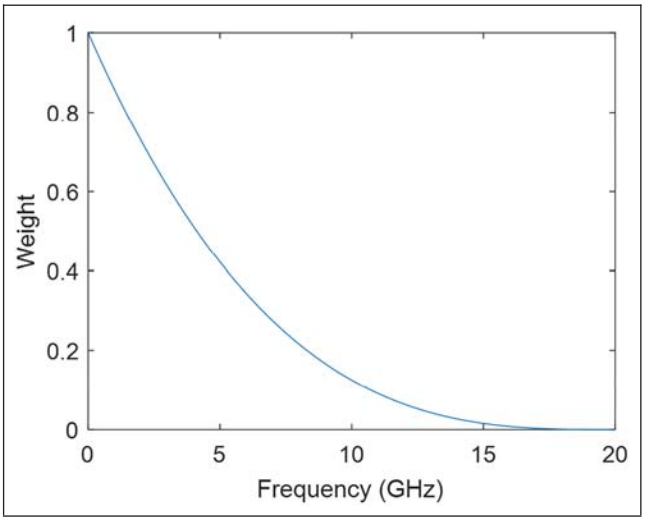

Figure 5-3 The Suggested Weight Function for Insertion Loss Curve Fitting

Typical least mean square fit approach is applied to fit the weighted raw data to the target function. Figure 5-4 shows the fitted insertion loss curve for two measurement cases using the procedures described above.

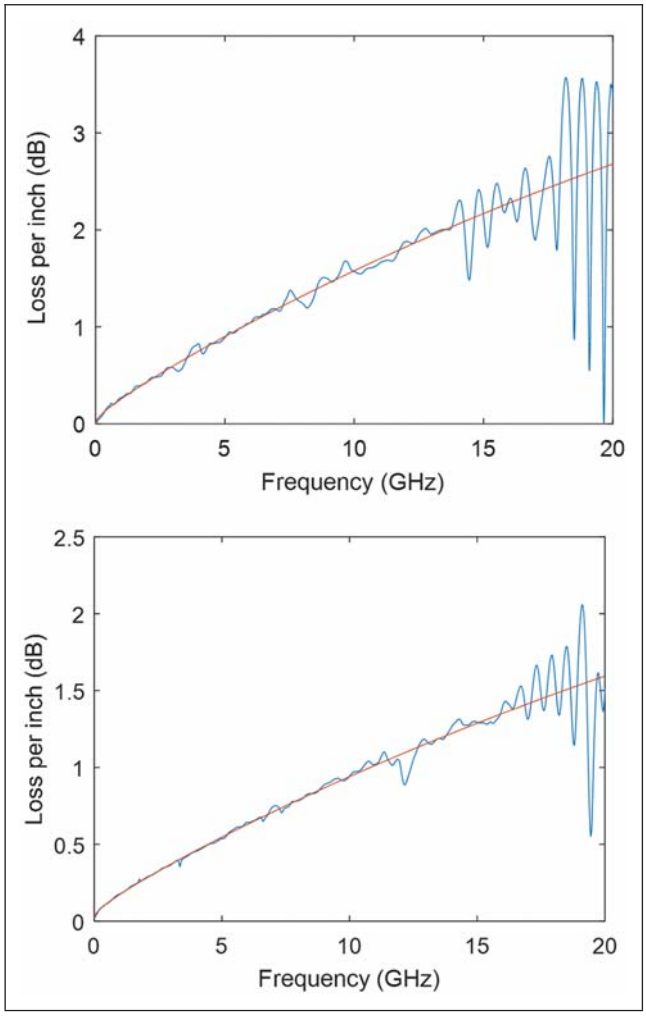

Figure 5-4 Examples of an Alternative Insertion Loss Fitting using Eq. 6

5.4.4 Addressing the Quality of Reported Insertion Loss As mentioned previously, when performing measurements on printed board conductors to check whether they pass insertion loss requirements, printed board testing houses generally only provide the insertion loss at a few points in their report. Usually, the reported loss value using the fitted value provides results with better fidelity compared to the raw data.

Meanwhile, the deviation of the reported values from the raw data is a good indicator on the quality of the measurement. The simplest approach to compute the uncertainty at the selected frequency is to use the difference between the raw data and fitted results. However, this can be misleading, which is demonstrated in Figure 5-5. In this case, the deviation of raw data from the fitted curve is zero at the selected frequency, while it is clear that the measurement quality is not perfect.

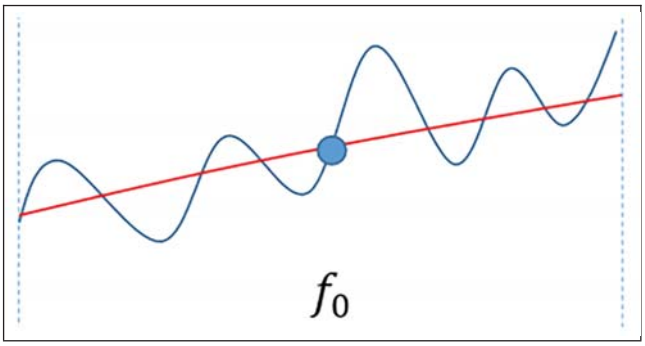

Figure 5-5 Deviation of the Raw Data from the Fitted Curve at a Single Frequency Point can be Misleading

To quantify the uncertainty of the reported insertion loss at the point of interest it is necessary to analyze the fit deviation in its immediate vicinity, as shown in Figure 5-5. An 'error neighborhood' of ± 1 GHz (can be adjust based on user's specific application) is suggested to calculate the fit precision using the distribution of the residuals within the ± 1 GHz frequency range. For frequency points at the lower or upper limit of the measurement bandwidth, the ± 1 GHz bound can be adjusted so that the 'neighborhood error bound' does not extend beyond the measurement bandwidth. For example, if the measurement upper frequency limit is 20 GHz, and the frequency of interest is 19.5 GHz, then the 'neighborhood error bound' is from 18.5 to 20 GHz.

From the fitted curve and the original raw data, the residuals, ILres(i) are calculated for all the frequency points within the ± 1 GHz range:

$$IL\_res(i) = IL\_raw(i) - IL\_fit(i) \quad \text{(Eq. 10)}$$

where IL_raw(i) is the raw data of insertion loss at each frequency points, and IL_fit(i) is the fitted insertion loss. The mean and standard deviation (σ) of the residual distribution is calculated, and the uncertainty at given frequency f0 is defined as:

$$uncertainty@f_0 = \frac{mean\ (IL_{\_res}) + 3 \times \sigma\ (IL_{\_res})}{IL_{\_fit}@f_0} \times 100\% \quad \text{(Eq.11)}$$

Note that an uncertainty estimate of 15% (as an example) is not meant to suggest that the true insertion loss is within 15% of the reported value. Rather, the uncertainty estimate is merely an indicator for the amount of measurement and de-embedding error evident at any given point.

5.4.5 Determine the Usable Bandwidth of Reported Insertion Loss The uncertainty level described in 5.4.4 can be used to determine the usable bandwidth of the reported insertion loss. The user can set up an acceptable uncertainty level based on a specific application, and then examine the reported insertion loss value at various frequencies, to determine its usable bandwidth of reported insertion loss (where the uncertainty level is smaller than the pre-set value).

5.5 Verification of Reported Insertion Loss Due to manufacturing variation, and the uncertainties associated with the calibration/de-embedding process, it is desirable to make multiple measurements of the same coupon design to improve the confidence of the measurement results. This is critical when the material is in a qualification stage and the amount of manufactured coupons is limited.

One simple approach to verify the reported insertion loss is to design coupons with multiple lengths on the same board: L1, L2, and L3. The de-embedding process outlined in 1.2.2 and 1.3 can be applied to any two length combinations:

$$IL_{unit\_12} = \frac{|e^{-\gamma(L2-L1)}|}{L2-L1} \quad \text{(Eq. 12)}$$

$$IL_{unit\_23} = \frac{|e^{-\gamma(L3-L2)}|}{L3-L2} \quad \text{(Eq. 13)}$$

$$IL_{unit\_13} = \frac{|e^{-\gamma(L3-L1)}|}{L3-L1} \quad \text{(Eq. 14)}$$

It is desirable to have the reported insertion loss per unit length being consistent (e.g., within 5% of each other). A large discrepancy indicates either problems in measurement/de-embedding procedures, or a large manufacturing variation across the board. An average of the above insertion loss number can be used to report the final value.

It is also important to note that keeping a large length difference between any two lengths among L1, L2, and L3 will also help to improve the quality of reported insertion loss.

5.6 Temperature Impact of Insertion Loss It is known that the copper conductivity decreases, and the loss tangent of dielectric material increases with the increase of environmental temperature. Therefore, the insertion loss increases with the increase of temperature. Meanwhile, the temperature impact on insertion loss varies with different printed board materials.

A Test chamber with variable temperature setting is needed. A suggested temperature range is 0 °C ~ +100 °C, or otherwise specified by the tester. Temperature accuracy is < ± 1 °C of actual set point. Humidity accuracy is < ± 5% RH of actual set point, or otherwise specified by the tester.

It is recommended to use phase-stabilized cables for temperature ranges of 0 °C ~ +100 °C, or otherwise specified by the tester. Figure 5-6 provides an example of a temperature experiment setup.

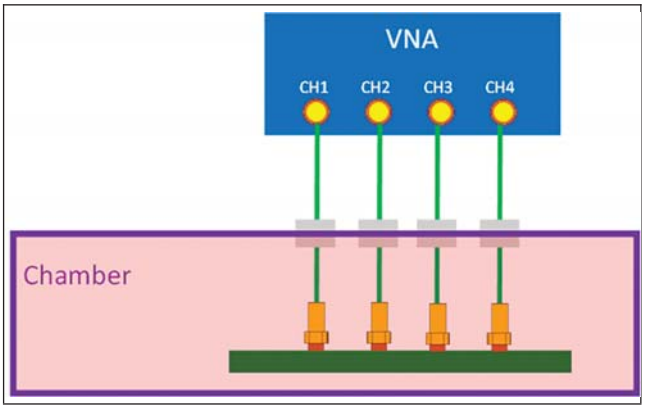

Figure 5-6 Temperature Experiment Setup

The following procedures describe how to quantify the temperature impact for a given printed board material:

1) Set up VNA equipment according to 5.1.
2) Bake the test coupon at 120 °C over 6 hours.
3) Calibration VNA equipment to the end of cable with co-axial connector SOLT standards, with the cable stayed outside the environment chamber.
4) Move cable end through the conduit of chamber and connect to the long trace of DUT inside the chamber. Make sure the conduit is sealed with thermal resistant material after the cable penetrates the chamber. (Note: high temperature resistant cable should be used)
5) Set the chamber to the target testing temperature and humidity.
6) Wait at least half an hour to ensure DUT is set to the ambient temperature
7) Conduct measurement and record data.
8) Moving to the next temperature and humidity setting (Step 5), until results of all settings are recorded.

9) Conduct the short trace characterization from Step 4.

10) Post-process the results using methods described in Section 1.2.2.

Note: The humidity is controlled at RH of 50% (±5%) for all data points, except for 0 and 100 °C.

5.7 Test Report Below is an example of the list of information to be included in the test report. The actual format and information to be included in the test report may vary based on the requirement of specific customer:

- VNA Settings: test frequency range, step size, IF bandwidth, etc.
- Probing method: handheld probe, microwave probe, or printed board mounted co-axial connector without probes
- Manufacturer and part number of the probe (if used), and the bandwidth of the probe per 4.2
- Condition of test samples per 3.8.1 or 3.8.2
- Temperature and humidity of testing condition for Room-Temperature test
- Temperature and humidity of testing condition for Varying-Temperature test per 5.6
- Calibration or de-embedding method per 1.2.2 or 1.3.1 or 1.3.2
- Insertion loss fitting method per 5.4.2 or 5.4.3
- Values of the insertion loss at test frequencies, in dB/inch or dB/cm
- Uncertainty estimate at test frequencies per 5.4.4
- Any anomalies in the test or variations from this test method

6 Reference Documents

[1] N. R. Franzen, R. A. Speciale, ''A New Procedure for System Calibration and Error Removal in Automated S-Parameter Measurements,'' Proceedings of the 5th European Microwave Conference, Hamburg, Germany, 1-4 September 1975, pp. 69-73.

[2] R. A. Soares, P. Gouzien, P. Legaud, G. Follot ''A Unified mathematical approach to two-port calibration techniques and some applications,'' IEEE Trans. on MTT, v. 37, N 11 1989, pp. 1669-1674.

[3] R. B. Marks, ''A Multiline Method of Network Analyzer Calibration,'' IEEE Transactions on Microwave Theory and Techniques 39, pp. 1205-1215, July 1991.

[4] C. Seguinot et al.: – Multimode TRL ''A new concept in microwave measurements''

[5] D. Degroot, J. Jargon, R. Marks, ''Multiline TRL revealed,'' 60th ARFTG Conference Digest, Fall 2002.

[6] Y. Shlepnev, ''Broadband material model identification with GMS-parameters'', 2015 IEEE 24th Conference on Electrical Performance of Electronic Packaging and Systems (EPEPS'2015), October 25-28, 2015, San Jose, CA.

[7] G. F. Engen and C. A. Hoer, ''Thru-Reflect-Line: An Improved Technique for Calibrating the Dual Six-Port Automatic Network Analyzer,'' Microwave Theory and Techniques, IEEE Transactions on, vol. 27, pp.987-993, 1979.

[8] V. Adamian, B. Cole, ''A Novel Procedure for Characterization of Multiport High Speed Balanced Devices,'' DesignCon, San Jose, CA, 2007.

[9] H. Barnes, E. Bogatin, J. Moreira, J. Ellison, et al. ''A NIST Traceable PCB Kit for Evaluating the Accuracy of DeEmbedding Algorithms and Corresponding Metrics,'' DesignCon 2018.

[10] X. Ye, J. Fan and J. Drewniak, ''New De-embedding Techniques for PCB Transmission-Line Characterization'', DesignCon 2015.

[11] IEEE P370 open-source 2X-Thru de-embedding code, https://gitlab.com/IEEE-SA/ElecChar/P370.

[12] https://standards.ieee.org/standard/370-2020.html

[13] S. Moon, X. Ye, R. Smith, ''Comparison of TRL Calibration vs. 2X-Thru De-embedding Methods,'' IEEE International Symposium on EMC and SI, 2015.

[14] A. Koul, M. Koledintseva, S. Hinaga, J. Drewniak, ''Differential Extrapolation Method for Separating Dielectric and Rough Conductor Losses in Printed Circuit Boards,'' IEEE Transaction on Electromagnetic Compatibility, Vol. 54, No. 2, April 2012.

[15] X. Ye, M. Balogh, ''Physics-Based Fitting to Improve PCB Loss Measurement Accuracy,'' IEEE International Symposium on EMC, 2017.